IN THE CLAIMS:

Please cancel claims 1, 6, 13 and 16 without prejudice or disclaimer, and amend claims 2, 7, and 18, as follows:

1. (Cancelled)

2. (Currently Amended) A semiconductor device ~~according to claim 1~~ comprising:

a first input/output interface circuit adapted to a serial bus;

an internal circuit for performing a circuit operation corresponding to a signal which is inputted or outputted through said first input/output interface circuit between said internal circuit and said serial bus;

a non-volatile storage circuit for storing identification data;

a comparator circuit for comparing internal identification data stored in said non-volatile storage circuit with external identification data included in an input signal supplied through said serial bus; and

a control circuit responsive to an input signal subsequently supplied through said serial bus when said comparator circuit generates a match detecting signal for performing a circuit operation corresponding to said input signal, wherein:

said internal identification data is read from said non-volatile storage circuit and transferred to a predetermined storage circuit under the condition that identification data stored in said non-volatile storage circuit transitions to a predetermined state.

3. (Original) A semiconductor device according to claim 2, further comprising:

a supply voltage detector circuit for receiving a power supply voltage, wherein:

said predetermined state is set when said supply voltage detector circuit detects that said power supply voltage rises to a first level.

4. (Original) A semiconductor device according to claim 2, wherein:

said predetermined state is set by a predetermined input signal which is first supplied through said serial bus after said semiconductor device is powered on.

5. (Original) A semiconductor device according to claim 2, further comprising a reset signal input terminal, wherein:

said predetermined state is set when a predetermined signal is inputted to said reset signal input terminal.

6. (Cancelled)

7. (Currently Amended) A semiconductor device ~~according to claim 6, further~~ comprising:

a first input/output interface circuit adapted to a serial bus;

an internal circuit for performing a circuit operation corresponding to a signal which is inputted or outputted through said first input/output interface circuit between said internal circuit and said serial bus;

a non-volatile storage circuit for storing identification data;

a comparator circuit for comparing internal identification data stored in said non-volatile storage circuit with external identification data included in an input signal supplied through said serial bus;

a control circuit responsive to an input signal subsequently supplied through said serial bus when said comparator circuit generates a match detecting signal for performing a circuit operation corresponding to said input signal;

wiring means adapted to said serial bus, said wiring means having one end connected to said first interface circuit;

a second input/output interface circuit connected to the other end of said wiring means; and

a signal processing circuit provided through said second input/output interface circuit, wherein:

said circuit operation performed by said control circuit includes: an operation for re-writing identification data into said non-volatile storage circuit in response to said input signal, and an operation directed to said internal circuit in response to said input signal,

said second input/output interface circuit and said signal processing circuit are mounted in a first semiconductor chip, and said first input/output interface circuit,

said internal circuit, said non-volatile storage circuit, said comparator circuit and said control circuit are mounted in a second semiconductor chip, and

said first semiconductor chip and said second semiconductor chip are integrally encapsulated into said semiconductor device.

8. (Original) A semiconductor device according to claim 7, wherein:

said wiring means comprises:

first bonding wires for connecting bonding pads corresponding to said second input/output interface circuit in said first semiconductor chip to associated leads; and

second bonding wires for connecting bonding pads corresponding to said first input/output interface circuit in said second semiconductor chip to associated leads.

9. (Original) A semiconductor device according to claim 8, wherein:

said signal processing circuit in said first semiconductor chip includes a processor unit, and a ROM for storing a signal processing procedure performed by said processor unit, and

said internal circuit in said second semiconductor chip includes a memory circuit which is allocated an address space difference from an address space allocated to said non-volatile storage circuit for storing said identification data.

10. (Original) A semiconductor device according to claim 9, wherein:

said memory circuit is comprised of memory cells each having the same structure as said non-volatile storage circuit for storing said identification data.

11. (Original) A semiconductor device according to claim 9, wherein:

said internal circuit comprises a CMOS circuit, and

said non-volatile storage circuit for storing said identification data is comprised of non-volatile memory cells in a single-layered gate structure formed by a manufacturing process used for manufacturing said CMOS circuit.

12. (Previously Presented) A semiconductor device, comprising:

a first input/output interface circuit adapted to a serial bus;

an internal circuit for performing a circuit operation corresponding to a signal which is inputted or outputted through said first input/output interface circuit between said internal circuit and said serial bus;

a non-volatile storage circuit for storing identification data;

a comparator circuit for comparing internal identification data stored in said non-volatile storage circuit with external identification data included in an input signal supplied through said serial bus;

a control circuit responsive to an input signal subsequently supplied through said serial bus when said comparator circuit generates a match detecting signal for performing a circuit operation corresponding to said input signal;

said circuit operation performed by said control circuit including:

an operation for re-writing identification data into said non-volatile storage circuit in response to said input signal; and

an operation directed to said internal circuit in response to said input signal;

wiring means adapted to said serial bus, said wiring means having one end connected to said first interface circuit;

a second input/output interface circuit connected to the other end of said wiring means; and

a signal processing circuit provided through said second input/output interface circuit, wherein:

said second input/output interface circuit and said signal processing circuit are mounted in a first semiconductor chip, and said first input/output interface circuit, said internal circuit, said non-volatile storage circuit, said comparator circuit and said control circuit are mounted in a second semiconductor chip;

said first semiconductor chip and said second semiconductor chip are integrally encapsulated into said semiconductor device;

said signal processing circuit in said first semiconductor chip includes a processor unit, and a ROM for storing a signal processing procedure performed by said processor unit;

said internal circuit in said second semiconductor chip includes a memory circuit which is allocated an address space difference from an address space allocated to said non-volatile storage circuit for storing said identification data;

said internal circuit comprises a CMOS circuit,

said non-volatile storage circuit for storing said identification data is comprised of non-volatile memory cells in a single-layered gate structure formed by a manufacturing process used for manufacturing said CMOS circuit;

said internal identification data includes first internal identification data and second internal identification data, wherein said comparator circuit and said control circuit compare third external identification data included in a first input signal supplied through said serial bus with said first internal identification data stored in said non-volatile storage circuit, and compare fourth external identification data included in said first input signal with second internal identification data stored in said non-volatile storage circuit when said first internal identification data matches said third external identification data, such that said control circuit enables an operation for changing said first internal identification data by a second input signal supplied subsequently to said first input signal through said serial bus under the condition that said second internal identification data matches said fourth external identification data.

13. (Cancelled)

14. (Previously Presented) A semiconductor device comprising:

an input/output interface circuit adapted to a serial bus;

an internal circuit for performing a circuit operation corresponding to a signal inputted or outputted through said input/output interface circuit between said internal circuit and said serial bus; and

a non-volatile storage circuit for storing identification data,

wherein the circuit operation performed by said internal circuit includes an operation for changing said identification data by an input signal supplied through said serial bus when an internal state transitions to a first state,

wherein said identification data includes first identification data and second identification data, wherein said internal circuit compares third identification data included in a first input signal supplied through said serial bus with the first identification data stored in said non-volatile storage circuit, and compares fourth identification data included in said first input signal with the second identification data stored in said non-volatile storage circuit when said first identification data matches said third identification data, such that said internal circuit transitions to said

first state under the condition that said second identification data matches said fourth identification data, and is permitted to perform an operation for changing said first identification data by a second input signal supplied subsequent to said first input signal through said serial bus.

15. (Original) A semiconductor device according to claim 14,

wherein said serial bus comprises an IIC bus.

16. (Cancelled)

17. (Previously Presented) A data processing system comprising:

a plurality of semiconductor devices, each said semiconductor device including:

an input/output interface circuit adapted to a serial bus;

an internal circuit for performing a circuit operation corresponding to a signal inputted or outputted through said first input/output interface circuit between said internal circuit and said serial bus; and

a non-volatile storage circuit for storing identification data;

wherein said internal circuit of each said semiconductor circuit performs an operation for changing said identification data by an input signal supplied through said serial bus when an internal state of said internal circuit transitions to a first state;

wherein said identification data of said each semiconductor device includes first identification data and second identification data, wherein said internal circuit of each said semiconductor device compares third identification data included in a first input signal supplied through said serial bus with the first identification data stored in said non-volatile storage circuit, and compares fourth identification data included in said first input signal with the second identification data stored in said non-volatile storage circuit when said first identification data matches said third identification data, such that said internal circuit transitions to said first state under the condition that said second identification data matches said fourth identification data, and is permitted to perform an operation for changing said first identification data by a second input signal supplied subsequent to said first input signal through said serial bus, so that different identification data are set in said respective semiconductor devices from one another.

18. (Currently Amended) A data processing system[[,]] according to claim 17, wherein: said serial bus comprises an IIC bus.